imperix

Written by: nicolas.cherix@imperix.ch
Revision/release date: Rev. B – Fri 29 Mar 2024

**PUBLIC DOCUMENT**

# INTERNSHIPS AND RESEARCH PROJECTS

**Written by:** Imperix ltd, Rte. des Ronquos 23, 1950 Sion, Switzerland
**Addressed to:** Any R&D-performing academic institution or industrial company

## SOFTWARE DEVELOPMENT PROJECTS

### USER EXPERIENCE DATA COLLECTION FOR SPECIALIZED NETWORKED HARDWARE

Motivations: Leverage user experience statistics in order to facilitate the continuous improvement of software products.
Objectives: Collect user experience data (e.g. user configuration, usage statistics, error logs, etc.) from embedded Linux and store it in the cloud.
Skills: Basic familiarity with Embedded Linux and Google Cloud is desired.

### FPGA DRIVER FOR THE GIGABIT ETHERNET MAC CONTROLLER OF A ZYNQ SOC

Motivations: Replace the current "Ethernet over RealSync" bridge, which runs on Linux, hence limiting the bandwidth and unnecessarily loading the CPU.
Objectives: Study how the PS Gigabit Ethernet MAC controller (GEM) operates and port part of the Linux Ethernet driver to the FPGA, redirecting the PS Ethernet (GEM) traffic.
Skills: Previous experience with embedded Linux and FPGA design is required.

### REDUNDANT COMMUNICATION FOR DISTRIBUTED CONTROL IN POWER ELECTRONICS

Motivations: The current implementation of "RealSync" doesn't offer any redundant mode.
Objectives: Study the possible types network redundancies and implement one. Investigate how to dynamically switch the reference clock for RealSync clock synchronization.
Skills: Previous experience with FPGA design is required.

### COMMUNICATION MANAGER – SUPPORT OF FIELD BUSSES FOR B-BOX RCP

Motivations: Improve or develop the support of CANopen, Modbus TCP, EtherCAT, and RS232 for imperix products.
Objectives: See motivations.
Skills: Some familiarity with embedded systems preferable. BSc level suitable.

### FLEXIBLE PERIPHERAL MANAGER FOR CODE GENERATION IN SIMULINK

Motivations: Validate the allocation of I/O and peripheral resources at the time of the automated generation of code (within Simulink) instead of at the code startup (in the target).
Objectives: Implement a flexible peripheral manager and adapt the hardware abstraction layer accordingly. Develop support for all three imperix programmable controllers.
Skills: Previous experience with Matlab Coder is a plus. BSc level suitable.

## AUTOMATED CODE GENERATION FOR MULTI-CORE SYSTEMS FROM SIMULINK

Motivations: Develop and evaluate the capability to automatically generate code for a multi-core system directly in Simulink.

Objectives: Design and implement the support for code generation for a multi-core system (Xilinx Ultrascale+, ARM Cortex-A53)

Skills: Previous experience with embedded systems is required. MSc level preferable.