Calculate and minimize the dead time for IGBTs

About this document

Scope and purpose

This application note describes how to measure the delay time of IGBTs and accurately calculate the control dead time based on these measurements.

Intended audience

This document is intended for all technical experts using Infineon power modules in various applications.

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1 Introduction

In modern industry, voltage source inverters with IGBTs are frequently used. To ensure their effective operation, bridge shoot-through should be prevented, since it generates additional losses, and may even cause thermal runaway. This in turn can lead to the failure of the IGBT devices, and the entire inverter.

1.1 Reasons for IGBT phase-leg shoot-through

Figure 1 depicts the typical configuration of a phase-leg setup with IGBTs. Two IGBTs are turned on and off successively in a regular operation. Both devices conducting at the same time will result in a rise of current limited mainly by the DC-link stray inductance.
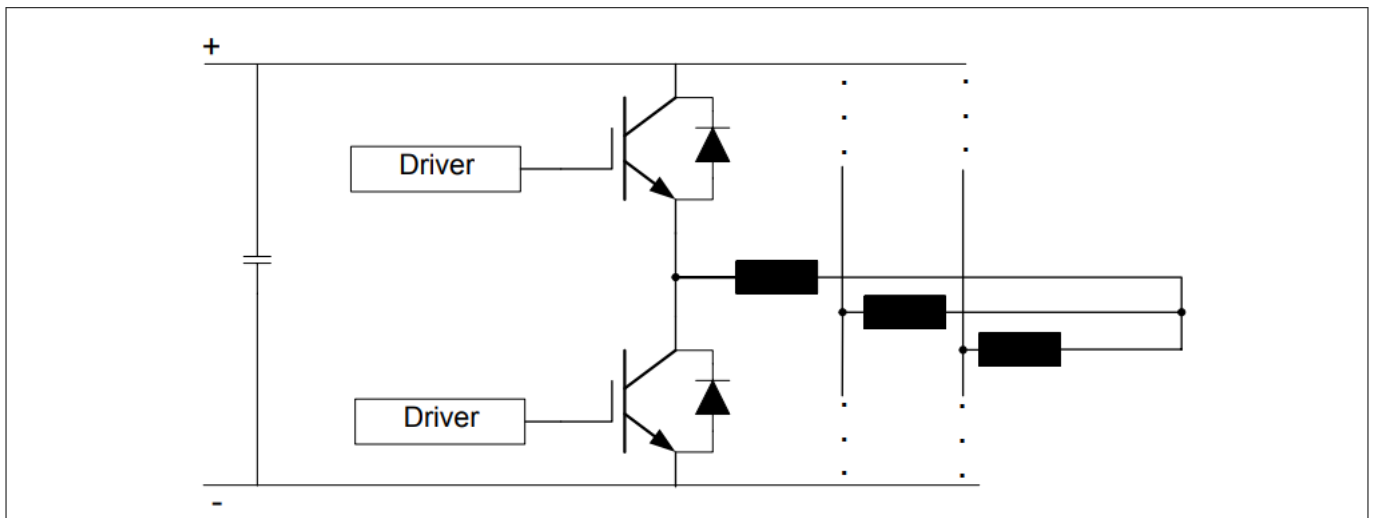

Figure 1   **Typical configuration of a voltage source inverter**

Although the two IGBTs are not intentionally turned on at the same time, the turn-on and turn-off times are not strictly identical, since the IGBT is not an "ideal" switch. To prevent the generation of a bridge shoot-through current, it is recommended to add a so-called "interlock delay time" or the more popular "dead time" into the control scheme. With this additional time, one of the two IGBTs is always turned off first, and the other one will be turned on after the dead time has expired, thus preventing a bridge shoot-through caused by the asymmetrical turn-on and turn-off times of the IGBTs.

1.2 Impact of dead time on inverter operation

There are generally two types of dead time: control and effective dead time. Control dead time is the time implemented in the control algorithm to achieve the desired effective dead time on the device. The purpose of setting a control dead time is to ensure that the effective dead time will have a positive value. Since control dead time is calculated on the basis of a worst-case analysis, there is an effective dead time that makes up a significant portion of the control dead time.

Although providing dead time can prevent bridge shoot-through, it also has some adverse effects. To illustrate the effect of dead time, consider the branching of a voltage source inverter, as shown in Figure 2. Assuming that the output current first flows in the direction shown in the figure, the IGBT T1 switches from ON to OFF, while the IGBT T2 switches from OFF to ON after a short dead time. During the effective dead time, both devices are turned off, and the freewheeling diode D2 conducts the output current. Applying negative DC-link voltage to the output is desirable here. Consider another case in which T1 switches from OFF to ON, and T2 switches from ON to OFF. With the output current flowing in the same direction, D2 still conducts the current during the dead time. Therefore, the output voltage is also a negative DC-link voltage, which is not desirable here. In conclusion, during the effective dead time, the output voltage is determined by the direction of the output current, but not by the control signal.

1 Introduction

Considering the output current is flowing in the opposite direction as that in Figure 2, the voltage will be obtained when T1 switches from ON to OFF, and T2 switches from OFF to ON. In general, applying dead time distorts the output voltage and the resulting output current. For an induction motor, selecting an unnecessarily long dead time can lead to system instability and catastrophic consequences [1]. Thus, the process of choosing a dead time is indispensable, and should be performed with caution.
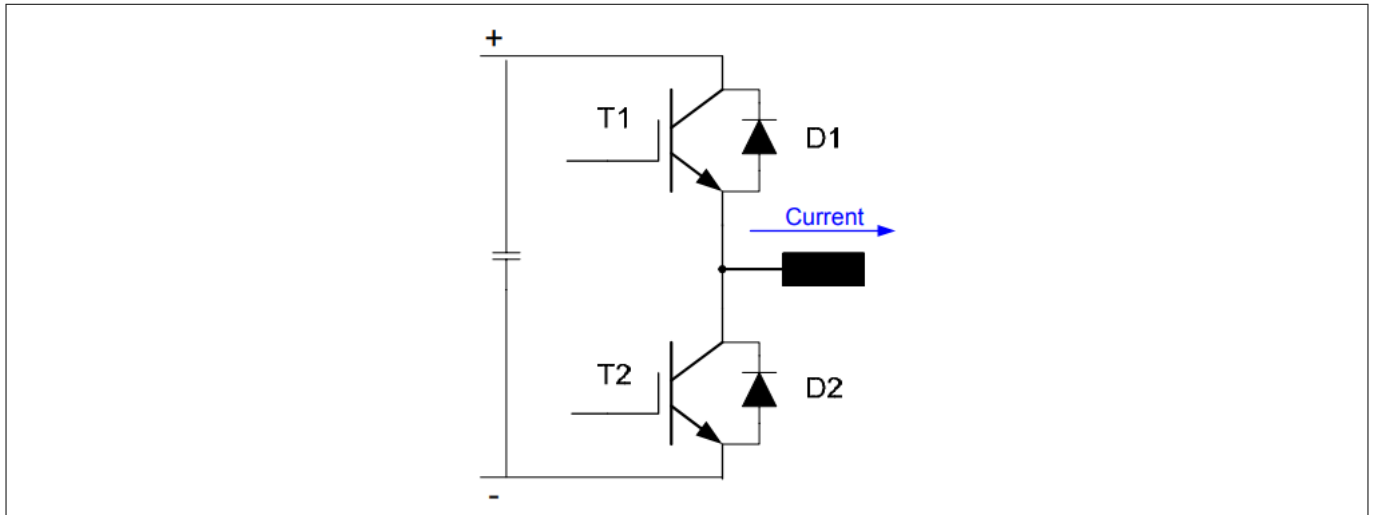
Figure 2   **A phase-leg of voltage source inverter**

2 Dead-time calculation

As mentioned, the dead time should be selected on the one hand to prevent shoot-through of the bridge, and on the other hand should be as short as possible to ensure the correct operation of the voltage source inverter. Thus, calculating the correct dead time for a dedicated IGBT device and driver is a challenge.

2.1 Basics of dead-time calculation

To calculate the control dead time, use the following equation:

$$t_{\text{dead}} = \left[\left(t_{\text{d\_off\_max}} - t_{\text{d\_on\_min}} \right) + \left(t_{\text{pdd\_max}} - t_{\text{pdd\_min}} \right) \right] \times 1.2 \tag{1}$$

Where,

- $t_{\text{d\_off\_max}}$ is the maximum turn-off delay time
- $t_{\text{d\_on\_min}}$, minimum turn-on delay time
- $t_{\text{pdd\_max}}$, maximum propagation delay of driver
- $t_{\text{pdd\_min}}$, minimum propagation delay of driver
- 1.2, safety margin value to be multiplied

In this equation, the first term $t_{\text{d\_off\_max}}$–$t_{\text{d\_on\_min}}$ is the difference between the maximum turn-off delay timeandthe minimum turn-on delay time. It describes the characteristics of the IGBT device controlled by its gate driver and gate resistor circuit. The fall and rise time is usually much shorter than the delay time and is not considered here. The second term, $t_{\text{pdd\_max}}$–$t_{\text{pdd\_min}}$ is the propagation delay time difference (delay time mismatch) determined by the driver. This parameter is usually found in the driver datasheet of the driver manufacturer.

At times, dead time is calculated by simply multiplying the values from the typical datasheet with a safety factor obtained from field experience. This method works in some cases, but is generally not accurate enough. The measurements shown here intend to provide a more precise approach.

Since the IGBT datasheet only lists typical values for standardized operating conditions, it is necessary to determine the maximum values for the operating conditions. For this purpose, a series of measurements are made to obtain the correct value for the delay time and then calculate the dead time.

2.2 Definition of switching and delay times

It is important to give a clear definition of the switching and delay times, as these terms will be discussed in detail in the subsequent chapters. The switching times of the IGBTs are defined as follows:

$t_{d(on)}$: from 10% of V_{GE} to 10% of I_C

t_r: from 10% of I_C to 90% of I_C

$t_{d(off)}$: from 90% of V_{GE} to 90% of I_C
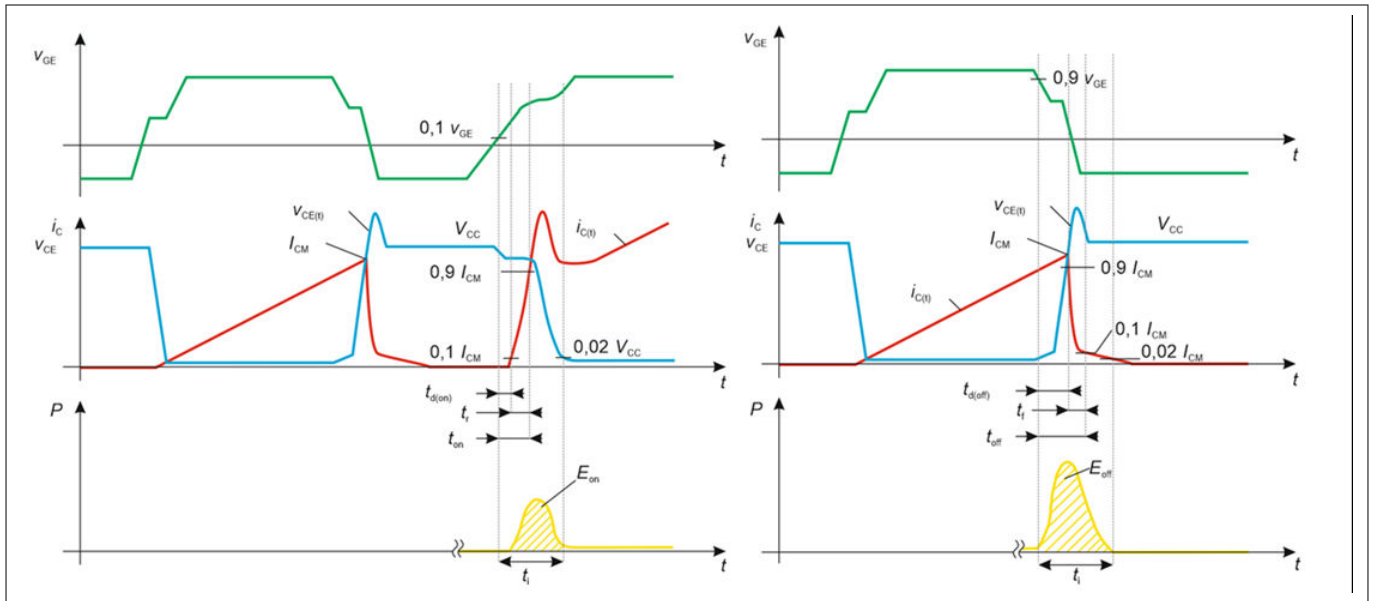
t_f: from 90% of I_C to 10% of I_C

Figure 3   **Definition of switching times**

2.3 Influence of gate resistor/driver output impedance

The choice of gate resistor has a significant effect on the switching delay time. In general, the higher the resistor, the longer the delay time. It is recommended to measure the delay time with a dedicated gate resistor in the application. Figure 4 and Figure 5 show the typical graphs of switching time versus gate resistor.
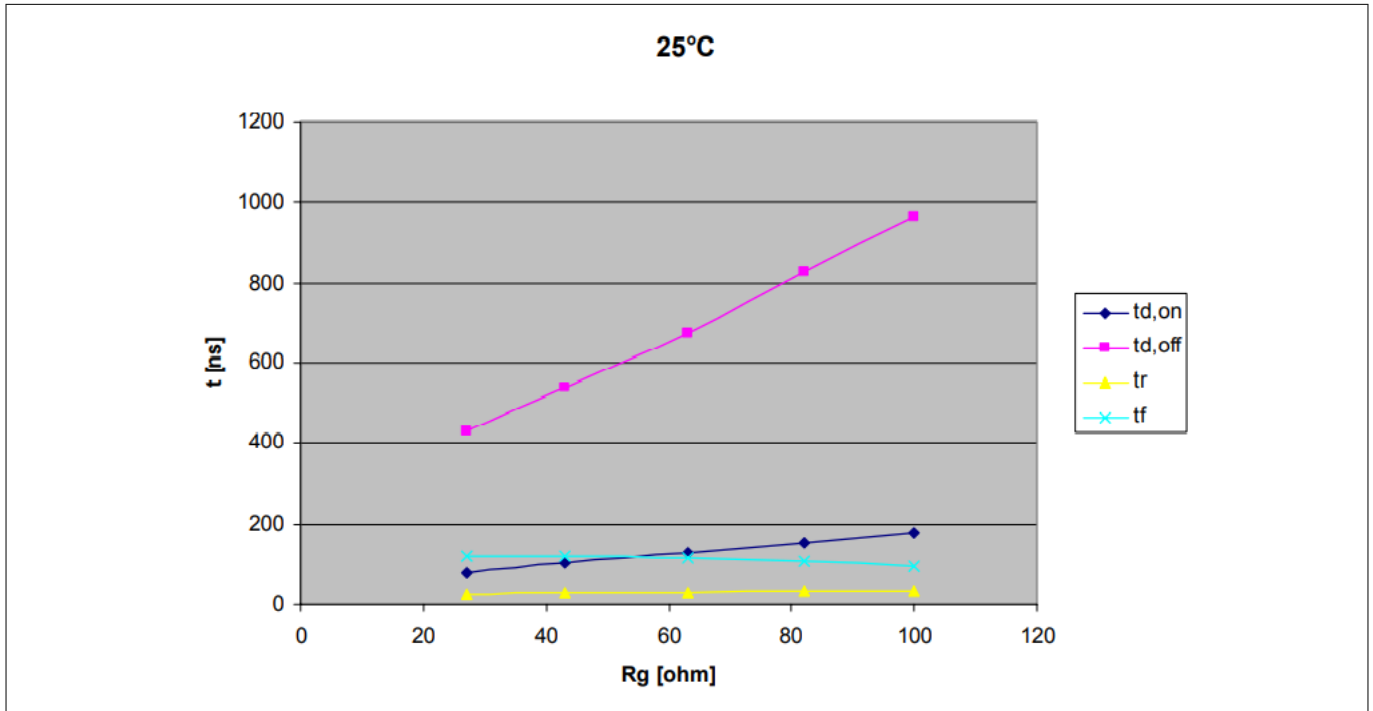

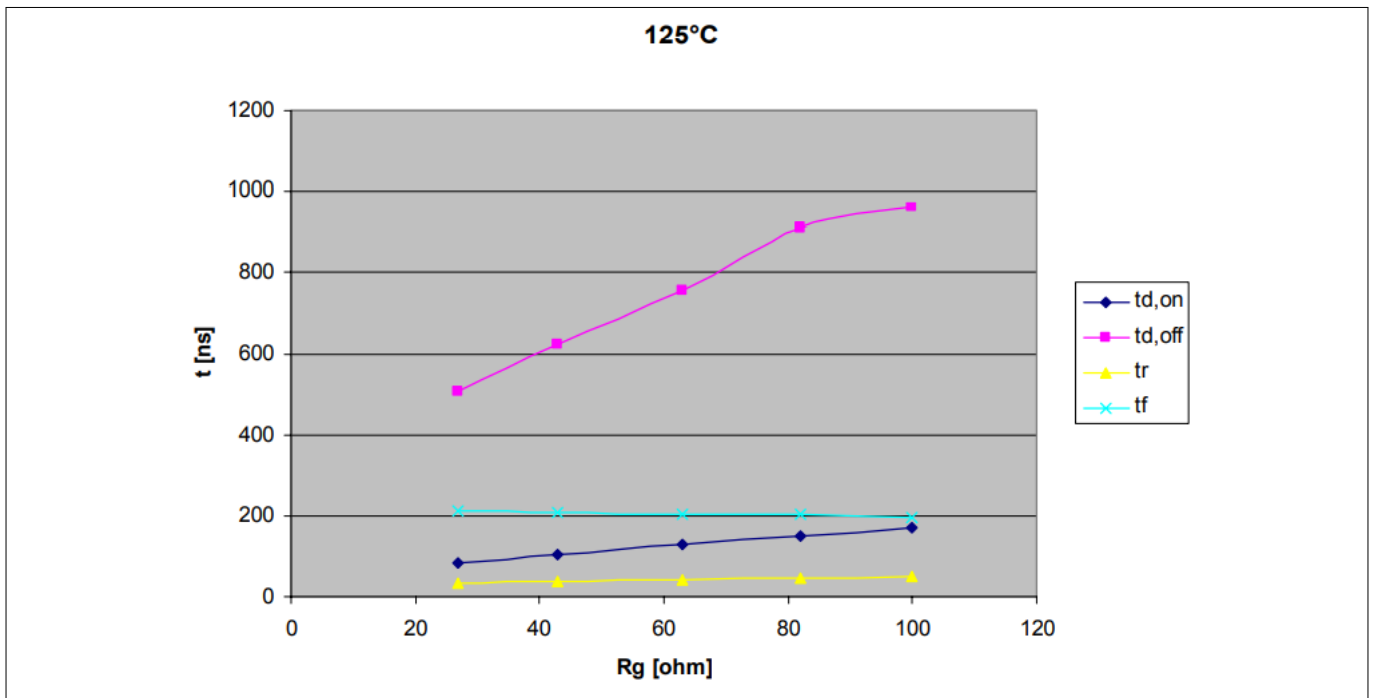**Figure 4   Switching times versus R_g at 25°C**

Figure 5   Switching times versus R_g at 125°C

Note: *All tests were performed using the FP40R12KT3 module with a gate voltage of –15 V/+15 V, a DC-link voltage of 600 V, and a switching current of 40 A nominal current.*

2.4 Impact of other parameters on delay time

In addition to the gate resistor values, the following parameters have a significant effect on the delay time:

- Collector current
- Gate driver supply voltage

2.4.1 Turn-on delay time

A series of measurements were performed to evaluate the relationship between delay time and current. First, the dependence of turn-on delay time and the current was investigated. Figure 6 shows the results.
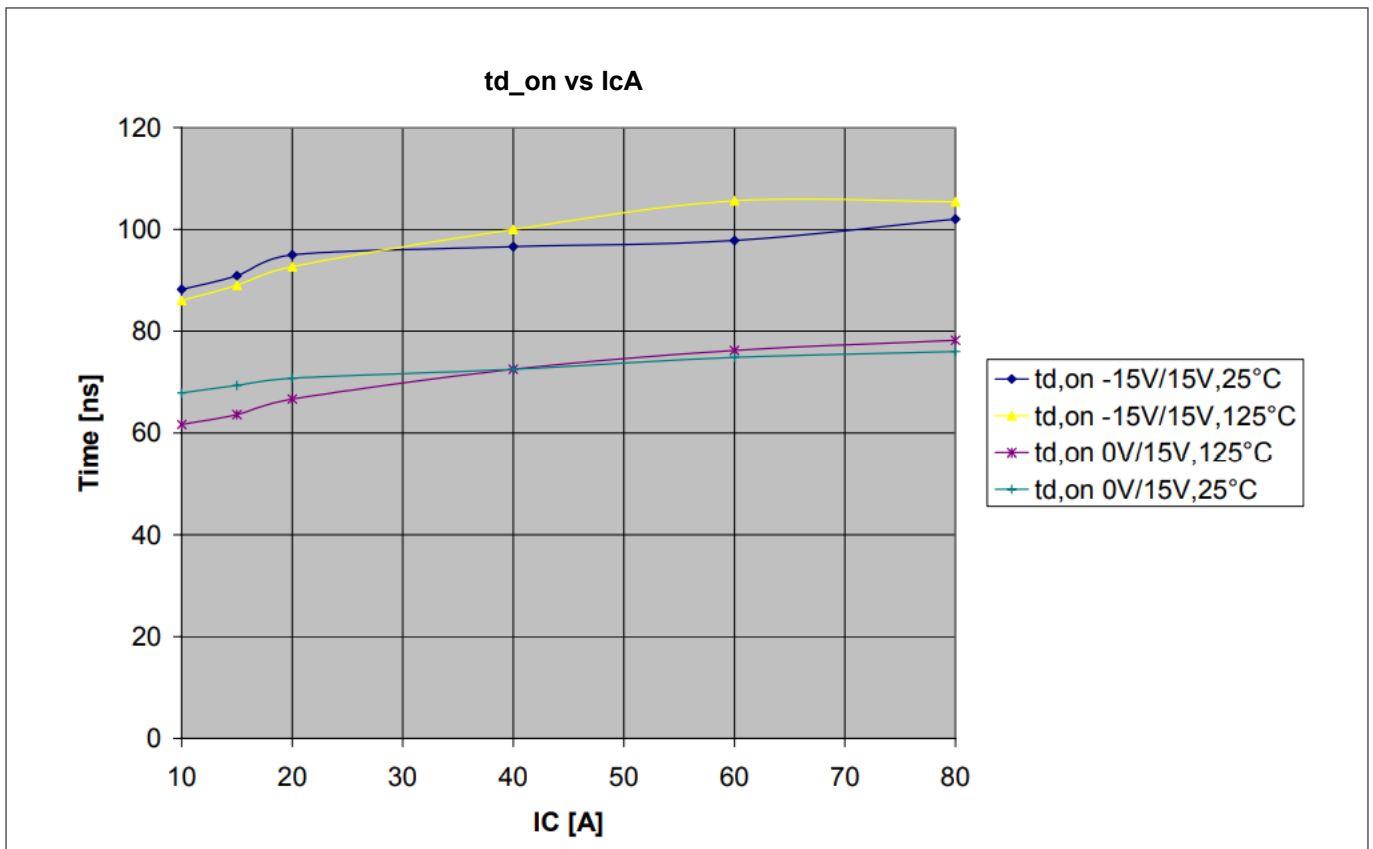

Figure 6   Turn-on delay time versus switching current I_C

Note: All tests were performed using the FP40R12KT3 module with a DC-link voltage of 600 V. The gate resistor is chosen based on the datasheet values.

In the results above, note that the turn-on delay time is almost constant with the variation of collector current I_C. For –15 V/+15 V gate voltage, the turn-on delay is longer when compared to 0 V/+15 V gate voltage [2]. This variation is negligible, and even provides an additional margin for further control dead -time calculation.

2.4.2 Turn-off delay time

The most significant factor in the calculation of dead time is the maximal turn-off delay time. This value determines the complete length of the final calculated dead time. An investigation of this delay time is detailed below.

To obtain the maximum turn-off delay time, the following conditions should be considered.

Steps

1. What is the duration of the turn-on delay time caused by the IGBT device itself?
   The test was performed based on the characterization driver board in the laboratory. The characterization driver board is considered as an optimal driver, which means that it will cause no delay (most likely for oversized drivers). Therefore, the entire delay time is attributed to the IGBT device itself. Figure 7 depicts the block diagram of the test setup.
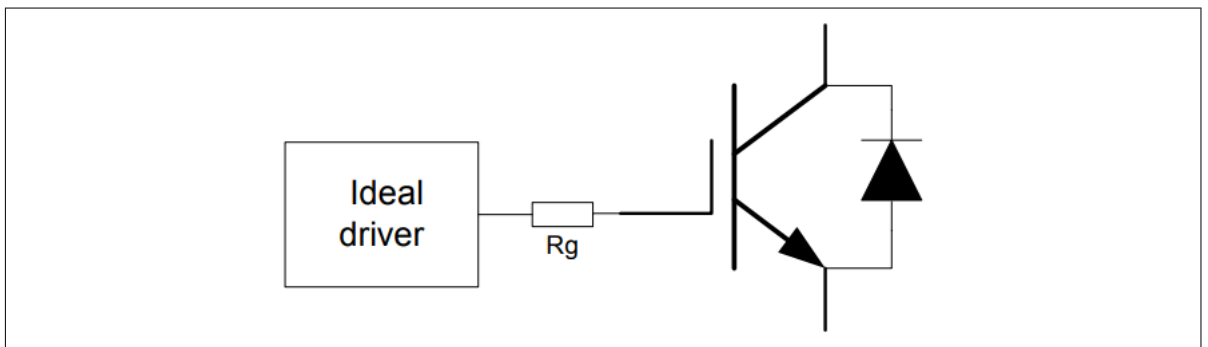

Figure 7   **Block diagram of a test with ideal driver**

2. What is the maximum turn-off delay time when the threshold voltage of the IGBT is at its minimum in the datasheet? (This reflects the Vth tolerance between modules.)
   Connect an additional diode to simulate a Vth voltage drop. The voltage drop of the diode is about 0.7–0.8 V, which is quite similar to the Vth variant of the FP40R12KT3 module. Figure 8 shows the block diagram of the principal test setup.
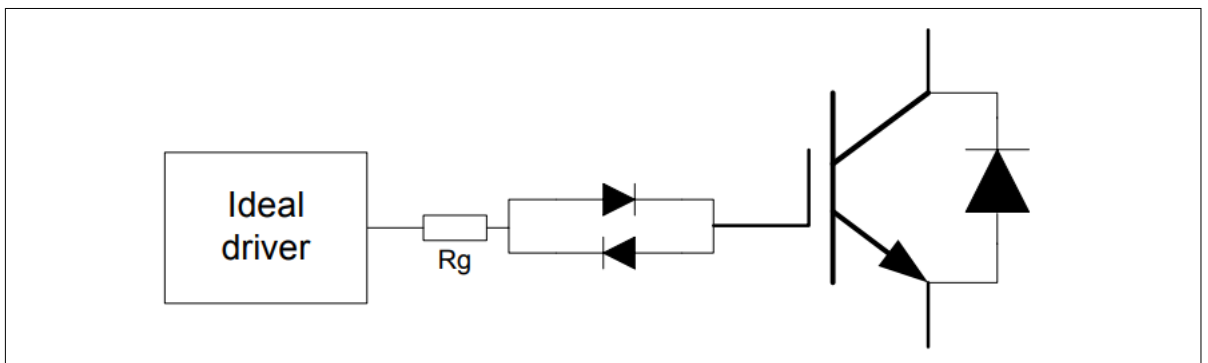

Figure 8   **Block diagram of a worst-case test that simulates Vth variation**

3. How does the driver output stage affect the switching time?
   The drivers in the market are divided into two categories: MOSFET transistor output stage and bipolar transistor output stage. For each category, individual measurements are made. An additional resistor is connected to simulate the driver with a MOSFET output stage. This resistor is considered as the on-state resistor $R_{ds(on)}$ of the MOSFET transistor. The diode for simulation of Vth variation remained. Figure 9 illustrates the block diagram of the principal test setup.
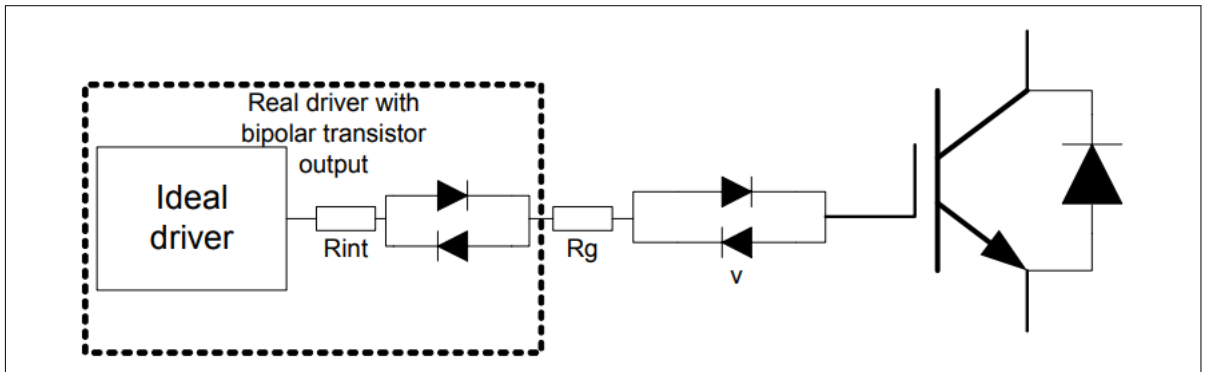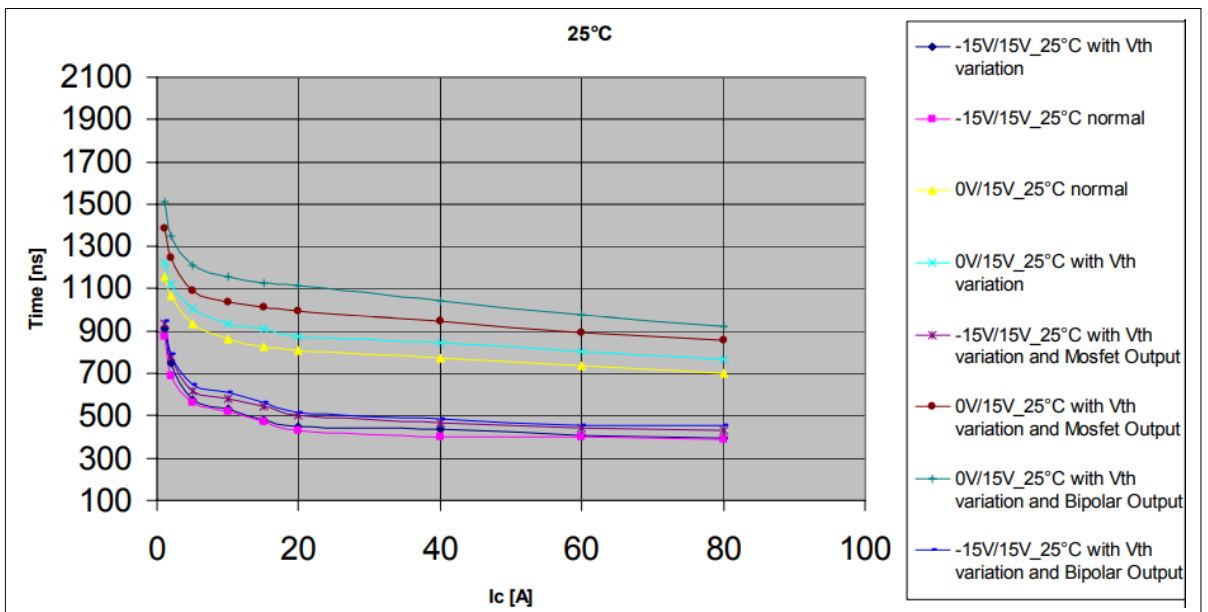
2 Dead-time calculation
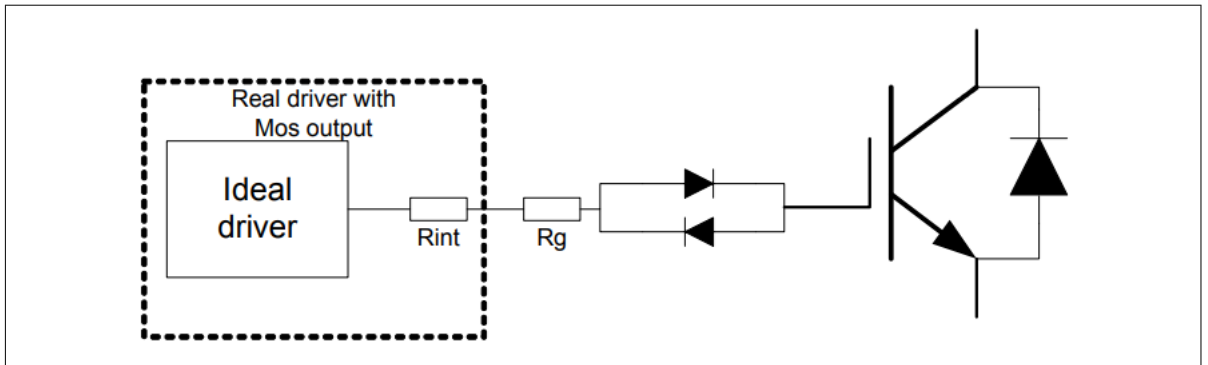
Figure 9   **Block diagram of a test that simulates Vth variation and driver with MOSFET output**

4.   What is the impact of the driver with bipolar transistor output stage?
Connect an additional diode to simulate a voltage drop across the bipolar transistor in the output stage.
Figure 10 shows the block diagram of the principal test setup.

Figure 10   **Block diagram of a test that simulates Vth variation and driver with bipolar transistor output**

In the above configuration, the measurement of turn-off delay time was performed in our laboratory using the FP40R12KT3 module, and the driver board that was considered optimal. The test conditions are: V_{dc} = 600 V and R_g = 27. Figure 11 and Figure 12 depict the results.

Figure 11   **Turn-off delay time versus I_C at 25°C**
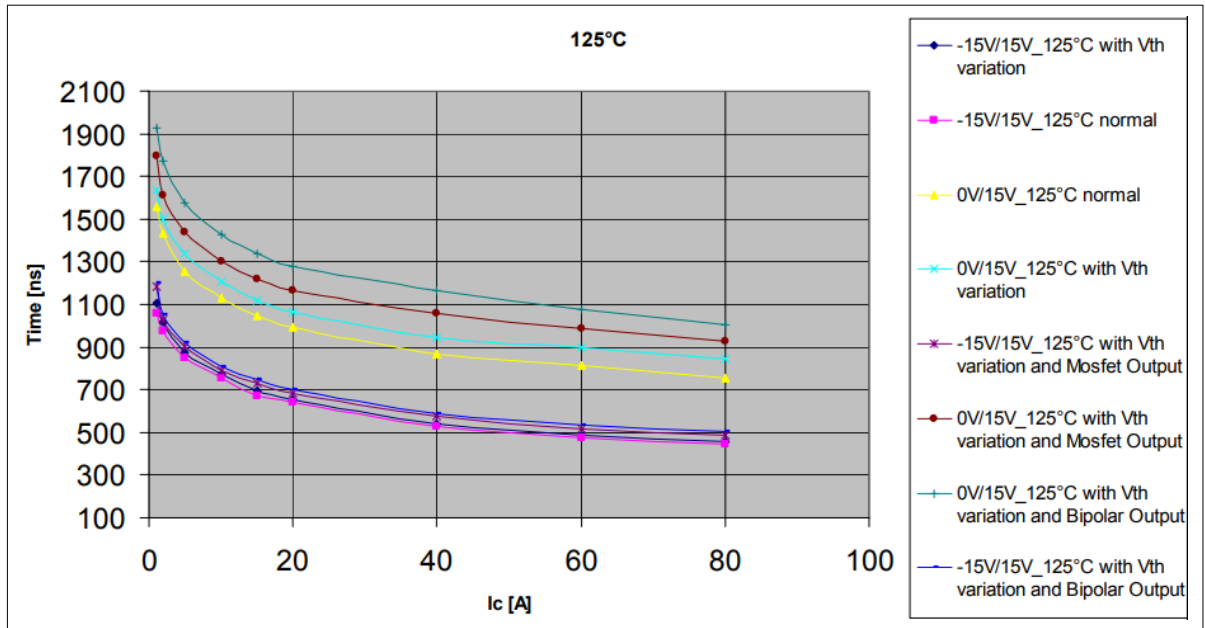
2 Dead-time calculation

Figure 12   Turn-off delay time versus I_C at 125°C

The results show that there is a significant increase in the turn-off delay time with the decrease of the switched current I_C. A simple calculation of dead time depending on the chosen gate resistor is not precise enough. It is more appropriate and accurate to measure the delay time under the actual driving conditions than to calculate the dead time based on these values. Measurement of up to 1% of the nominal current is adequate to provide a sufficient overview for calculating the required dead time.

Another point to consider is that the turn-off delay time increases with the 0 V/+15 V gate driver, and the impact of the output stage on the switching time with 0 V/+15 V switching increases. This means that with a switching voltage of 0 V/+15 V, special care should be taken when choosing a driver. In addition, the increase in t_{d_off} when the switched collector current I_C is low should also be considered.

Example

Consider the HCPL-3120 driver IC that has a MOSFET output stage for switching off. From the above figures, the value of t_{d_off} under the switching condition of 0 V/+15 V is about 1500 ns. In this case, t_{d_on} is about 100 ns. According to the datasheet, $t_{pdd\_max}-t_{pdd\_min}$ for this driver IC is 700 ns. Applying these values to equation (1) results in a dead time of approximately 2.5 μs.

2.4.3 Verification of calculated dead time

Based on the measurements discussed in Chapter 2.4 and equation (1) in Chapter 2.1, it is possible to calculate the required dead time. Using this calculated dead-time, you can perform a worst-case measurement to verify if the selected dead time is sufficient.

Measurements show that the turn-off delay time increases with temperature. For this reason, the test is performed preferably under both low- and high-temperature conditions. Figure 13 represents the schematic diagram of the test.
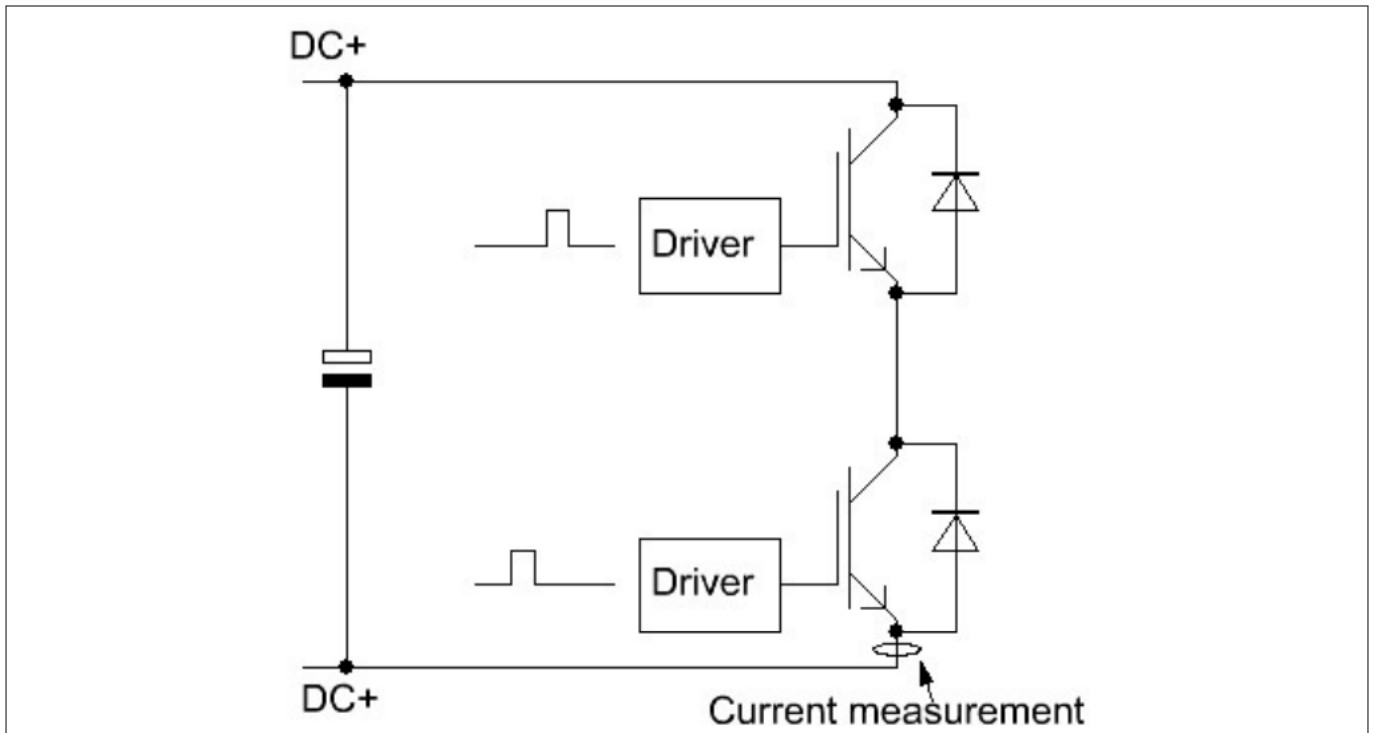
Figure 13   Schematic diagram of the test to verify the calculated dead time value

The lower IGBT has to be switched ON and OFF, followed by the same procedure for the upper IGBT. The time between the two pulses should be adjusted to the value of the calculated dead time for the dedicated driving condition. The negative DC-link current can then be measured, and as a result, a shoot-through current should not be observed if the dead time is sufficient.

The test described represents the worst-case condition for a dead-time calculation, as there is no current flowing through both IGBTs. The description of the turn-off delay time shows that the dead time increases with the decrease of the collector current. Therefore, the turn-off delay time should be maximized when no current is flowing, which in turn requires a maximum dead time. If there is no shoot-through current when the collector current is zero, the selected dead time is sufficient for a dedicated driving condition.

3 Dead time reduction

For a precise calculation of the control dead time, consider the following driving conditions:

- What is the applied gate voltage to the IGBT?
- What is the chosen gate resistor value?
- What type of output stage does the driver have?

Based on these conditions, perform a test and calculate the control dead time from the test results using equation (1).

Since dead time affects the inverter performance, it should be kept to a minimum. Several methods are available, some of which are listed below:

- Choose a driver that is powerful enough to lower or generate peak IGBT gate current
- Use a negative power supply to accelerate turn off
- Prefer drivers based on high-speed signal transmission technologies, such as the coreless transformer technology, over those based on the traditional optocoupler technology
- Use a separate R_{gon}/R_{goff} resistor for a 0 V/15 V gate driver as described below

From the measurements shown in Chapter 2.3, a very strong dependence on T_{d_off} and the gate resistor value is observed. As R_{goff} decreases, both t_{d_off} and dead time decrease. It is recommended to reduce the value of R_{goff} to one-third of the R_{gon} value when a gate voltage of 0 V/15 V is used. Figure 14 shows a possible circuit for separate R_{gon} and R_{goff} values.
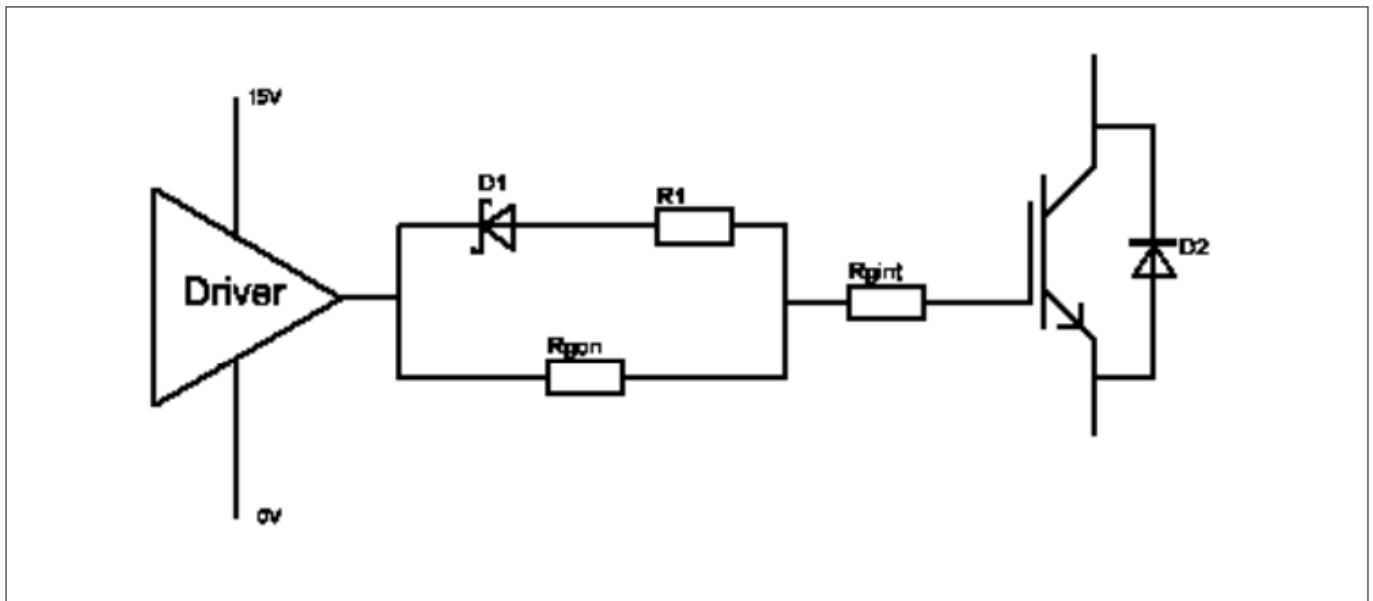

Figure 14   **Suggested circuit with 0 V/15 V gate voltage**

The resistor R_1 is chosen to satisfy the following relation:

$$\frac{R_1 \cdot R_{gon}}{R_1 + R_{gon}} + R_{gint} = \frac{1}{3} \cdot \left(R_{gon} + R_{gint} \right) \tag{2}$$

$$\Rightarrow R_1 = \frac{1}{2} \cdot R_{gon} \cdot \frac{R_{gon} - 2R_{gint}}{R_{gon} + R_{gint}} \tag{3}$$

3 Dead time reduction

From equation (3), note that the condition $R_{\text{gon}} > 2R_{\text{gint}}$ must be met to obtain the positive value of R_1. However, some modules do not meet this requirement, in which case R_1 can be omitted completely.

Attention**: **The diode must be a Schottky diode.

Another significant issue with the 0 V/15 V gate voltage is the parasitic switch-on effect. It can also be resolved by using the proposed circuit.

Note: *For more details on the parasitic turn-on effect, please refer to AN2006-01* [2].

4 Conclusion

This document presents an approach for measuring IGBT switching time and calculating the control dead time. It also describes the dependence of the switching time on the gate resistor value, the effect of the gate driver and collector current on the switching time, and finally, a possible way to reduce the dead time.

References

[1]   D. Grahame Holmes, Thomas A. Lipo: *Pulse width modulation for power converters: principles and practice*; IEEE Press, 2003; ISBN 0-471-20814-0

[2]   *Infineon Technologies AG: Driving IGBTs with unipolar gate voltage*; http://www.infineon.com/dgdl/an-2006-01_Driving_IGBTs_with_unipolar_gate_voltage.pdf?folderId=db3a304412b407950112b408e8c9000 4&fileId=db3a304412b407950112b40ed1711291

Revision history

Document version	Date of release	Description of changes
V1.0	2007-04	Initial version
V1.10	2021-12	New format, Changing Fig. 3

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